REMARKS/ARGUMENTS

Applicants request an interview with the Examiner to discuss this response.

Applicants amend claim 9 to change "at leas tone" to "at least one" to overcome the Examiner objection on pg. 2 of the OA1. Claims 21 and 37 were similarly amended

Claims 13, 22, and 26 are amended to remove limitation reference numerals.

Claims 10, 2, and 38 are amended to remove an extraneous instance of "and" between limitations.

Claim 31 is amended to depend from claim 30.

1. Amended Claim 11 Complies with 35 U.S.C. §112, par. 1

The Examiner rejected claim 1 as failing to comply with the enablement requirement (35 U.S.C. §112, par. 1) on the grounds the Specification does not adequately disclose the claimed "local memory information". (OA1, pgs. 2-3). Applicants traverse with respect to amended claim 11.

Applicants amend claim 11 to add punctuation to clarify that information is written to the local memory by reciting "writing, to the local memory, information". Thus, the amended claim does not recite an element "local memory information", but instead recites that said information is written to the local memory. Applicants submit that this claim requirement is disclosed in at least FIG. 8, block 170 and paras. 32 and 33 of the Specification. For instance, para. 33 discloses "information the packet processing block 104 writes to the local memory 6."

Applicants further amend claim 11 to change "memory" to "local memory".

Applicants note that the Examiner said he would interpret claim 11 as amended. (OA1, pg. 4)

Applicants submit that this amendment overcomes the enablement rejection on the grounds the Specification discloses a local memory, to which information is written. Accordingly, Applicants request that the Examiner withdraw this rejection in view of this amendment.

Applicants further amended claims 23 and 39, which include substantially the same limitations of claim 11 in system and article of manufacture form, to include the clarification amendments made to claim 11.

2. Amended Claim 11 Complies with 35 U.S.C. §112, par. 2

The Examiner rejected claim 11 as indefinite (35 U.S.C. §112, par. 2) on the grounds the language "local memory information" is unclear.

Applicants amend claim 11 as discussed to clarify that the information is written to the local memory. Applicants submit that this clarification amendment overcomes the indefiniteness rejection. Applicants made similar amendments to claims 23 and 39.

Applicants request the Examiner to withdraw the indefiniteness rejection in view of this amendment.

3. Claims 1-25 and 29-40 are Patentable Over the Cited Art

The Examiner rejected claims 1-25 and 29-40 as obvious (35 U.S.C. §103) over Hassan (U.S. Patent No. 7,280,542) in view of Boivie (U.S. Patent No. 7,079,501), Verplanken (U.S. Patent No. 6,038,592), and Tsuchiya (U.S. Patent Pub. No. 2002/009396). Applicants traverse for the following reasons.

Claims 1, 13, and 29 require receiving a multicast packet to transmit to destination addresses; writing a payload of the multicast packet to at least one packet entry in a packet memory; generating headers for the destination addresses; generating at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses; and generating, for each destination address, at least one indicator including information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor.

The Examiner cited col. 11, lines 44-48 and FIG. 5 of Hassan as teaching the claim requirement of generating at least one descriptor addressing the at least one packet entry in the packet memory including the payload to transmit to the destination addresses. (OA1, pg. 5, 23-24, 41-42) Applicants traverse.

The cited col. 11 mentions that a linked buffer 510 includes an index relating to a leaf and root flow index values and a pointer containing pointers to the cell memory locations. The root cells are stored or written too using the root index as they are enqueued for MC (multicast) service. The cell memory effects MC scheduling operations. Although the cited Hassan discusses cell memory locations, the Examiner has not cited where Hassan teaches or suggests

the claimed descriptor addressing at least one packet entry in the packet memory including the payload to transmit to the destination address. The Examiner has not cited where Hassan teaches that the cell memory locations comprise or include a descriptor addressing a packet entry including the payload to transmit to the destination addresses. Accordingly, the cited col. 11 of Hassan does not teach generating at least one descriptor as claimed.

The Examiner cited col. 11, lines 25-28 and 44-48 and FIGs. 4 and 5 of Hassan as teaching generating, for each destination address, at least one indicator including information on the generated header for the destination address and the at least one descriptor, wherein indicators for the destination addresses address the at least one descriptor. (OA1, pgs. 5-6, 23-24, 41-42) Applicants traverse.

The cited col. 11 mentions that for the MC scheduling operations, leaf index values correspond to N leaf flows associated with a root flow. A linked buffer has an index portion relating to the leaf and root flow index values and a pointer location portion pointing to the cell memory locations, having cells enqueued for an MC service. Hassan mentions that in the MC flow arrangement, a root flow is transmitted to a plurality of egress interfaces using leaf flows, and that a scheduler implements the MC scheduling activity. (Hassan, col. 9, lines 13-25)

Although the cited Hassan discusses a multicast (MC) flow, there is no teaching of the claim requirement that an indicator is generated for each destination address including information on a generated header for the destination address and at least one descriptor that addresses at least one packet entry including the payload for the destination address. The Examiner has not cited where Hassan' teaches that its MC scheduling operations using leaf nodes performs the claim operations of generating for each destination address an indicator which includes information on the header for the destination address and a descriptor , where the descriptor addresses a packet entry in a packet memory including the payload to transmit to the destination address.

Further, the cited Hassan does not teach that indicators for the destination addresses address the at least one descriptor, meaning multiple indicators for different destination addresses address the same descriptor.

Thus, although the cited Hassan discusses a leaf and root flow for multicast scheduling, it does not teach or suggest the specific claim requirements of generating a descriptor and

generating for each destination address an indicator as claimed. Thus, the cited Hassan fails to teach or suggest the claim requirements for which it was cited.

The Examiner cited col. 7, lines 1-8, 20-21, and 33-34 of Verplanken as teaching generating an indicator including information on a message. (OA1, pgs. 7, 25, 43) Applicants note that claims 1, 13, 26, and 29 do not recite this language, and instead recite "generating, for each destination address, at least one indicator including information on the generated header and the at least one descriptor". The cited Verplanken does not teach or suggest the claimed indicator.

The cited col. 7 of Verplanken mentions that a buffer chaining control block (BCCB) which contains information relating to buffer chaining in a message and a message chaining control block (MCCB) containing information relating to the message chaining. An offset field indicates the beginning of the data in the buffer and a message count field gives the number of bytes used in the message.

Although the cited Verplanken discusses information maintained for a message, this does not teach generating an indicator for each destination address having information on a generated header for the destination address and at least one descriptor, where each descriptor addresses a packet entry having the payload. Further, the cited Verplanken does not teach that indicators for the destination addresses address the at least one descriptor, meaning multiple indicators for different destination addresses address the same descriptor.

The Examiner did not cite Boivie and Tsuchiya to address the above discussed shortcomings of Hassan and Verplanken with respect to the claim limitations for which they were cited.

Thus, even if one were to combine the teachings of the different references as the Examiner proposes, the cited combination does not render obvious claims 1, 13, and 29 because the cited combination does not teach or suggest all the claim limitations for which it is recited. Accordingly, claims 1, 13, and 29 are patentable over the cited combination.

Claims 2-12, 14-25, and 30-40 are patentable over the cited art because they depend from one of claims 1, 13, and 29, respectively. Further, the following dependent claims provide additional grounds of patentability over the cited art for the following reasons.

Claims 2, 14, and 30 depend from claims 1, 13, and 29, respectively, and further require that the payload is written to multiple packet entries in the packet memory, wherein one

descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted

The Examiner cited the above discussed col. 11 as teaching the claim requirement that one descriptor is generated for each packet entry including the payload, and wherein one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted (OA1, pgs. 8-9) Applicants traverse.

The cited col. 11 mentions that for the MC scheduling operations, leaf index values correspond to N leaf flows associated with a root flow. A linked buffer has an index portion relating to the leaf and root flow index values and a pointer location portion pointing to the cell memory locations, having cells enqueued for an MC service. Hassan mentions that in the MC flow arrangement, a root flow is transmitted to a plurality of egress interfaces using leaf flows, and that a scheduler implements the MC scheduling activity. (Hassan, col. 9, lines 13-25)

Although the cited Hassan discusses a multicast (MC) flow, there is no teaching of the claim requirement that one descriptor is generated for each packet entry including the payload and that one indicator is generated for each descriptor and destination address to which the payload in the packet entry addressed by the descriptor is transmitted. The cited node flows of Hassan do not teach or suggest that there is one indicator for each destination address and descriptor generated for one packet entry.

The cited Verplanken does not address the above discussed deficiencies of Hassan.

Accordingly, claims 2, 14, and 30 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited combination of references.

Claims 6, 18, and 34 depend from claims 1, 13, and 29, respectively, and further require using, for each destination address and indicator associated with the destination address, the information on the generated header in the at least one indicator for the destination address to access the header for the destination address; and transmitting, for each destination address and indicator associated with the destination address, the payload from the entry in the packet memory associated with the indicator and the accessed header for the destination address.

The Examiner cited co. 9, lines 12-16 and FIGs. 1 and 4 of Hassan and col. 7, lines 1-8, 20-21, and 33-34 of Verplanken as teaching the requirements of these claims. (OA1, pgs. 12-13,) Applicants traverse.

The cited Hassan mentions a multicast (MC) flow arrangement where a root flow entering an ATM switch is transmitted to a plurality of egress interfaces using corresponding leaf flows. The cited Verplanken mentions a buffer chaining control block (BCCB) which contains information relating to buffer chaining in a message and a message chaining control block (MCCB) containing information relating to the message chaining. An offset field indicates the beginning of the data in the buffer and a message count field gives the number of bytes used in the message.

Nowhere do the cited Hassan and Verplanken teach or suggest that for each destination address and indicator associated with the destination address, information on the header in the indicator is used for the destination address to access the header. The Examiner has not cited where Hassan or Verplanken teach that an indicator associated with a destination address, which addresses a descriptor, is used to access the header for the destination address.

Accordingly, claims 6, 18, and 34 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited combination of references.

Claims 10, 22, and 38 depend from claims 1, 13, and 29, respectively, and further require writing to a local memory at least one handle for each destination address addressing the at least one indicator for the destination address; writing the handles in the local memory to an output queue; and queuing the indicators corresponding to the handles in the output queue to at least one packet queue.

The Examiner cited col. 8, lines 3-5 and 58-60, col. 12, lines 37-39 and 50-56, and FIGs. 5, 9 of Verplanken as teaching the additional requirements of these claims. (OA1, pgs. 18-19, 37, 55)

The cited col. 8 mentions that free indirect control blocks (ICBs) are gathered in a free indirect control queue and that a DSI may read the address of the next direct control block to a corresponding buffer. The cited col. 12 mentions that in multicast processing, data buffers stored in a data structure in a data store represent a message and that it is not necessary to store the

address of the next message, and the directory control blocks may be stored in the CBS and that the indirect control blocks point to the original control block via the MCCB pointer.

Although the cited Verplanken mentions how to store a message, there is no teaching or suggestion of the claim requirement of writing to a local memory a handle for each destination address that addresses an indicator for the destination address, that the handles are queued in an output queue, and that the indicators corresponding to the handles are queued in a packet queue in the output queue. The Examiner has not cited where Verplanken teaches the use of two different queues, one to store handles for each destination address and the other to queue indicators corresponding to the handles in the output queue. Instead, the cited Verplanken mentions buffers and a data structure representing a message. The specific claimed indicators, handles, output queue and packet queue are not taught or suggested in the cited combination.

Accordingly, claims 10, 22, and 38 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not taught or suggested in the cited combination of references.

4. Claims 26-28 are Patentable over the Cited Art

The Examiner rejected claims 26-28 as obvious over Hassan in view of Boivie, Verplanken, Tsuchiya and Mamillapalli (U.S. Patent Pub. No. 2005/0111452). Applicants traverse.

Claim 26 substantially includes the requirements of claims 1, 13, and 29 and additionally recites a switch fabric and a plurality of line cards coupled to the switch fabric, wherein each line card includes a network processor, wherein each network processor includes a packet memory; and circuitry in communication with the packet memory that performs the operations recited in claims 1, 13, and 29.

The Examiner cited the above discussed combination of references with respect to the requirements of claim 26 common to claims 1, 13, and 29. (OA1, pgs. 59-63) Accordingly, claim 26 is patentable over the cited art for the reasons discussed above with respect to claims 1, 13, and 29.

Claims 27 and 28 are patentable over the cited art because they depend from claim 26, which is patentable over the cited art for the reasons discussed below.

Conclusion

For all the above reasons, Applicant submits that the pending claims 1-40 are patentable. Should any additional fees be required beyond those paid, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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